UTIRAC: University of Tokyo infrared array control system developed for WINERED

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ABSTRACT

We are developing a 2K × 2K format array control system (**UTIRAC**: University of Tokyo InfraRed Array Control system) for *"WINERED"*, which is a new high-resolution ($R_{max} = 100,000$) near-infrared (0.9-1.35 μm) spectrograph being built at the Institute of Astronomy, University of Tokyo. *UTIRAC* has the following two characteristics: (1) applicable to various infrared array (with Amp-ADC integrated boards which enables easy increase/decrease of the number of input channels) and (2) based on the MESSIA5 system (for clock generation and frame acquisition) developed by National Astronomical Observatory of Japan. The goals of *UTIRAC* are low readout noise (< 10 e$^-$) and readout speed of 200 kHz/pix (for the Raytheon *VIRGO* array). Working tests of each board and integration test with MESSIA5 system have been completed. As a next step, we are going to test *VIRGO* MUX for operation 4 with outputs and to evaluate readout noise. In the near future, we will increase the number of input channels on a single Amp-AD board from one to four for the operation of arrays with 16 outputs.

Keywords: near-infrared, array controller, VIRGO, HgCdTe, WINERED, spectroscopy, high dispersion

1. INTRODUCTION

We have been developing a 2K × 2K format array control system (**UTIRAC**: University of Tokyo InfraRed Array Control system) for "*WINERED*[1–4]", which is a new high-resolution ($R_{max} = 100,000$) near-infrared (0.9-1.35 μm) spectrograph being built at the Institute of Astronomy, University of Tokyo. See Ikeda et al.[1] and Yasui et al.[2] in this volume for the details of *WINERED*. Because of the high spectral resolution ($R > 28,000$), it is possible to obtain spectra between sky OH airglow lines and the sky background is negligible. Also, the ambient thermal background is negligible because *WINERED* wavelength range is limited to the short near-infrared (Figure 1). Therefore, the development of low readout noise system is very critical for the sensitivity of *WINERED*

Recently, several near-infrared 2K×2K detector arrays have been developed (see e.g., a review article by Finger & Beletic[5] 2003). Especially, Rockwell 2.5 μm HgCdTe HAWAII-2 detector arrays are widely used and the HAWAII-2 array control systems have been developed also in Japan for several Subaru instruments such as MOIRCS[6] and FMOS.[7] On the other hand, Raytheon 2.5 μm HgCdTe "*VIRGO*" detector array is becoming popular in the astronomical community (see e.g., VISTA program[8]). In Japan there are growing needs for the array control system for the *VIRGO* array. Therefore we started to develop an array control system that can be used for various 2K×2K infrared arrays.

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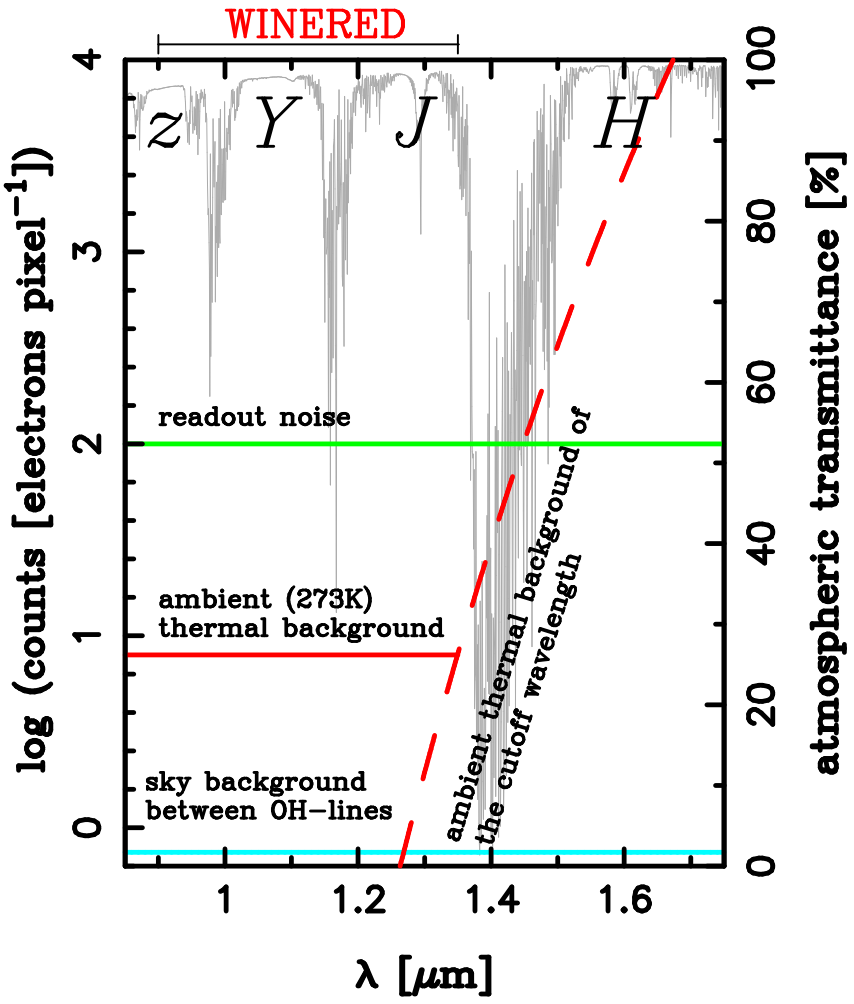

Figure 1. A comparison of the three background levels, -readout noise of the array readout system, ambient thermal background, and sky background between OH airglow lines in the wavelength range covered by *WINERED* The horizontal axis shows the wavelength and the vertical axis shows the electron count rate. The dashed line shows the ambient thermal background if the cut-off wavelength is set as the wavelength. The top horizontal solid line shows the background level equivalent to the readout noise that is assumed to be $10\,\mathrm{e}^-$ rms pix^{-1}. The middle and bottom horizontal solid lines show levels of ambient thermal background (at 273 K) with 1.35 μm cut-off and sky background between OH airglow lines, respectively. There are calculated assuming a telescope diameter of 6.5 m, a slit width of 0".3 and an integration time of 1800 s. The ambient thermal background is assumed to enter the detector pixel ($20\mu\mathrm{m} \times 20\mu\mathrm{m}$) as f/2 beam. Because of the high spectral resolution ($R > 28,000$), it is possible to obtain spectra between sky OH airglow lines. In the short near-infrared regions (z,Y, and J band), both backgrounds are negligible as compared to the readout noise. The thin lines show the atmospheric transmittance.

2. ARRAY CONTROL SYSTEM

UTIRAC is a new control system for 2K×2K format infrared arrays. As shown in Figure 2, this system consists of two parts: (1) front-end analog section and (2) cPCI-based digital section based on MESSIA5[9] system, which is developed by National Astronomical Observatory of Japan. The front-end analog section consists of six types of boards: fanout board, which is installed in the cryostat, Amp-AD board, clock driver board, bias board, isolator board, and power board. All the boards except the fanout board are based on the Euro card VME-3U size and installed in the rack a where signals are transmitted over the back plane. The analog data signals from the fanout board are transmitted over coaxial flat cables to the Amp-AD boards in differential signal for low

readout noise. Because Amp and ADC are installed on a single board, it is easy to increase and decrease the number of input channels according to the number of the array output channels: this extensibility is the major characteristic of *UTIRAC* to improve the system extensibility. The specification of *UTIRAC* is summarized in Table 1 and its block diagram is Figure 2.

Table 1. The specifications of *UTIRAC*

Items	Specification
Minimum clock pulse width	70 nsec
Pixel rate	200 kHz /pix /ch
Front-end circuit noise	<1 least significant bit
Conversion gain	3.0-6.0 e^-/ADU
Readout noise	< 10 e^-rms/pix

2.1. Infrared Array

VIRGO array[10,11] is the primary candidate for *WINERED*. *VIRGO* is a 2048×2048 format HgCdTe array detector with 20 μm pixel scale with high quantum efficiency over the wavelength range from 0.85 to 2.5 μm. The *VIRGO* ROIC (Readout Integrated Circuit) utilizes a PMOS source follower per detector input circuit with a well capacity of about 2×10^5 e^- and with a read noise of less than 15 e^- rms/pix. *VIRGO* has 16 or 4 output channels, and a frame rate of up to about 1.5/0.38 Hz in 4/16 output modes. To operate this array, we need 2 clocks (master clock and frame start clock), 3 control lines (selection of the number of output channels and reset mode), 13 bias lines, and 2 current sources, which can be replaced by DC bias lines for the operation. Raytheon Co. has kindly loaned a *VIRGO* multiplexer (MUX) to us and we are about to test *UTIRAC* with it (Figure 3).

2.2. MESSIA5 System

MESSIA5[9] system is used as the digital section of *UTIRAC*. MESSIA5 works for both clock generation and data acquisition. We summarize MESSIA5 system in the following.

- Hardware

  The hardware of MESSIA5 system consists of MESSIA5 Common Mezzanine Card (MESSIA5 CMC), DSP board (BittWare Sharc PCI Board) on CompactPCI, and a cPCI host PC based on Linux OS. MESSIA5 CMC is composed of Clock Sequencer Block (CSB) and Frame Grabber Block (FGB). CSB has one 32 bit clock output port and FGB has one 16 bit image-data input port. CSB accepts clock patterns from the DSP board and transmits it to the front-end electronics. FGB accepts 16 bit data and transmit it to frame memory of DSP board, which finally transmits it to the host PC.

- Software

  We have newly developed the MESSIA5 software for *VIRGO*. The functions of software are: (A) generation of clock pattern and (B) data acquisition.

  (A) Generation of Clock Pattern

  Clock pattern is defined in two files, "cpg.ascii" and "spv.ascii". "cpg.ascii" is minimum unit file of clocks, in which bit patterns of clocks are written. "spv.ascii" defines clock pattern combination of bit patterns as defined in "cpg.ascii". These clock patterns are loaded to DSP board, and transmitted over MESSIA5 CMC to front-end electronics.

  To operate *VIRGO* and acquire frame data with this system, the following 12 clocks are required.

  (a) Main Clock

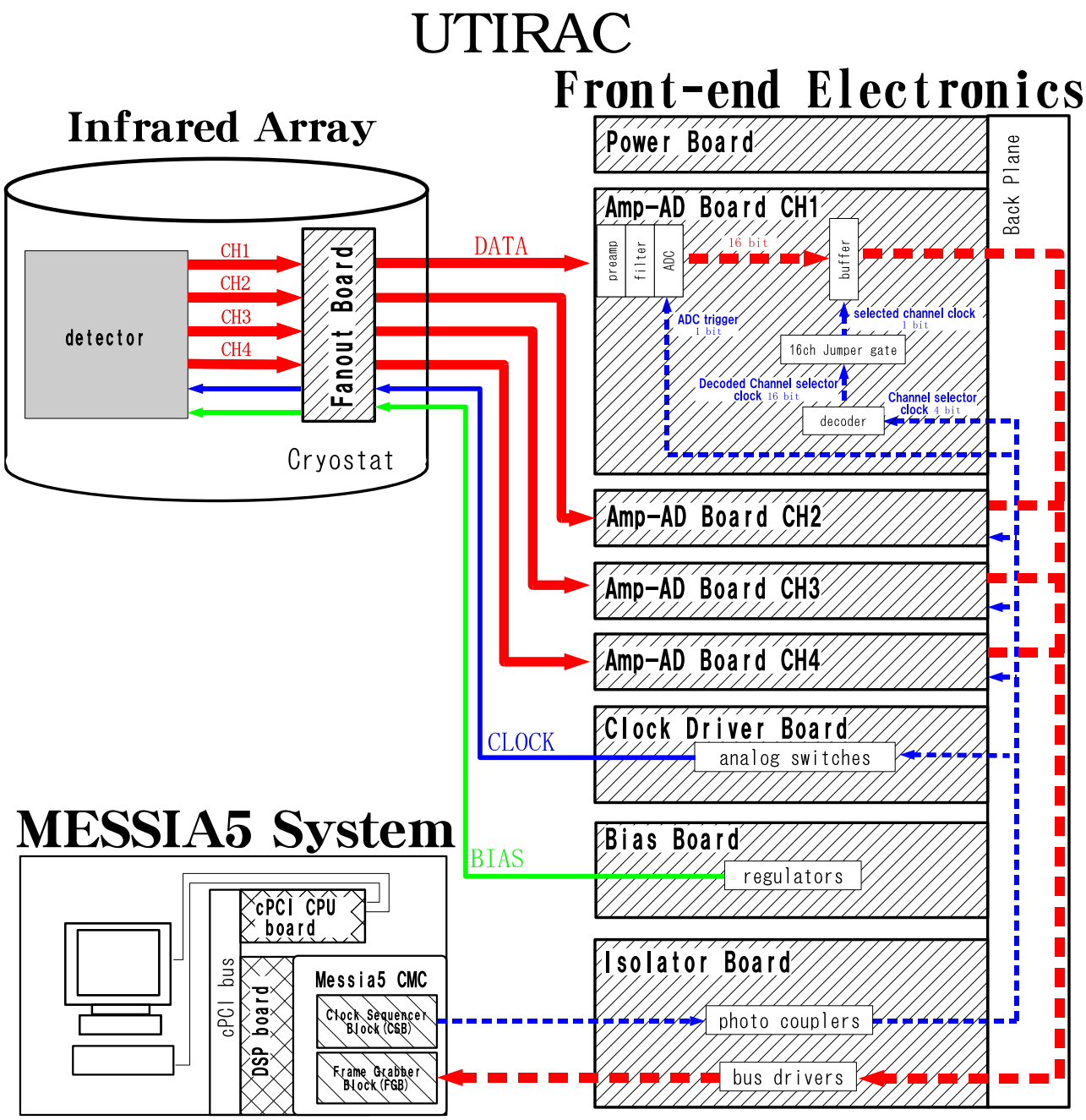

Figure 2. Block diagram of *UTIRAC*, which consists of the front-end electronics and the MESSIA5 system. The current Amp-AD Board has only one input channel for testing purpose. We will increase the number of input channel from one to four.

- FrameStart: Start read operation.
- pmc: The master clock with 200 KHz cycle.
  Only two clocks are required to run the *VIRGO*: CMOS logic circuit in the MUX generates all the clocks needed to operate the row and column shift registers and control the reset operation. To readout the full array, at least 2050 rows must be read. The first row output is a reference

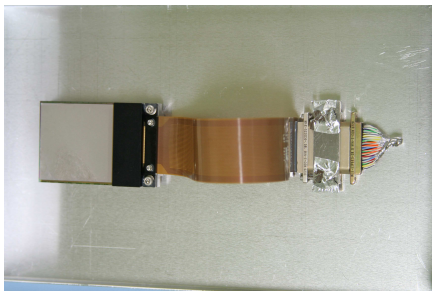

Figure 3. The *VIRGO* MUX on loan from Raytheon.

where all pixels are held at reset. The second row contains image data form row 1. Each row is 134 pixel long in 16 output mode and 518 pixel long in 4 output mode.

(b) Control Line

- reduceOut: Select the number of outputs (4 or 16).
- ucRstSel: Select global or row reset.
- ucRstEn: Enable the unit cell reset for a frame.
  The readout configuration of *VIRGO* is electrically controlled via three input control lines. The readout latches the state of these three signals on the next rising edge of the master clock after the FrameStart is received.

(c) Front-end Clock

- Trigger: The trigger of ADC.
- Select1∼4: Select ADC output channel transmitted to MISSIA5 CMC.
  These clocks are for Front-end electronics.

(d) Frame Gate Clock

- SCLK: Enable data input.
- Load: The trigger of 16 bit data input.
  These clocks are for loading data to FGB and not transmitted to the front-end electronics.

(B) Data Acquisition

The following procedure is used.

1. Assurance of memory region in the host PC.
2. Start readout clock. The data is written in the frame memory on DSP with DMA.
3. Transmit data in the frame memory to the main memory on the host PC with DMA after readout has finished.
4. Rearrange pixel data with reference to the MAP table:
   Because pixel data of 4/16 outputs of *VIRGO* are sent out in parallel, the raw image data on memory is a mixture of quadrants. The MAP table specifies the destination address of the final image pixel data.
5. Save the data as FITS format.

2.3. Front-end analog section

Front-end analog section consists of a fanout board in the cryostat and front-end electronics which consist of five types of boards. We explain the detailed functions of each board in the following. The pictures of each board are shown in Figure 4.

- In the cryostat
  - **Fanout Board**

    This board is installed in the cryostat ($\sim$ 80K) receives analog signals from the array detector, and transmits these signals over coaxial flat cables to the Amp-AD boards. The resistors to drive the output source follower are implemented on this board. A reference voltage used for differential signal output is produced also. Clocks and DC biases are received from the front-end electronics and are transmitted to the detector. DC biases are filtered by RC low-pass filters employing the OS-con (SANYO Electric Co.), which has a large capacitance, low Equivalent Series Resistance (ESR), and long life.

- Front-end Electronics
  - **Amp-AD Board**

    The differential signals of each input channel from the fanout board are transmitted to the instrumental amplifier (INA111, Bur Brown Corporation), which has high common-mode rejection of 106 dB min, with a gain of 10.1. Then the signals are filtered by Bessel low-pass filters with a gain of 1.27 and a cut-off frequency of 528 kHz determined by the readout speed of *VIRGO*, and are digitized by 16-bit A/D converters (AD7671, ANALOG DEVICES). As a result, the total conversion gain is 3.0-6.0 e^-/ADU. These digital data are transmitted to the isolator board through the data bus, controlled by 16-bit buffers/drivers with 3-state outputs (SN74ABT162244, Texas Instruments). Each channel of every board has an ID number and 16-bit digital data of only the selected channel are transmitted to the isolator board. Clocks of Select1$\sim$4(4-bit) are decoded to 16-bit by the decoder (CD74HCT154, Texas Instruments) to select the channel*.

    Because Amp and ADC are installed on a single board, we can easily increase and decrease the number of input channels just by changing the number of boards. Though the current board has only one input channel for the testing purpose, the number of input channels on one board will be increased to four to reduce the number of boards in the near future.
  - **Isolator Board**

    This board receives 18-bit clock signals sent from the CSB of MESSIA5 CMC by way of photo-couplers (HCPL-2430, Hewlett Packard), which electrically isolates the front-end electronics from the host PC. six bit clock signals are used for the front-end analog section; analog-to-digital conversion trigger and channel selection signals. Other 12-bit clock signals are available for the clock of the array detector. This board also receives 16-bit data from A/D converters and sends them to the FGB of MESSIA5 CMC by way of bus driver (LTC1688, LINEAR TECHNOLOGY) for isolation.
  - **Clock Driver Board**

    This board generates the clock signals of 0V and 4V, which controls *VIRGO*. Digital clock signals sent form the isolator board are converted to analog clock signals with analog switches (DG403, MAXIM). Each analog clock is buffered by Op-Amps to avoid interference. This board can provide 6 clocks, which is enough to drive *VIRGO*, which requires 5 clocks (2 clocks and 3 control lines). Maximum two clock driver boards can be installed to provide maximum 12 clocks. This board also supplies 3 and 4 V DC biases, which are digital biases for *VIRGO*.
  - **Bias Board**

    This board supplies max 10 different DC biases for the operation of *VIRGO*. While *VIRGO* requires current sources for the driver source followers (16 PMOS), they can be replaced by a combination of a DC bias and a resistor in the fanout board.
  - **Power Board**

    This board makes the DC powers which are isolated from outside DC power supplies and provides them to all the boards.

*The number of maximum input channels of *UTIRAC* is currently limited to 16 by the number of the selection clocks(4). The number of input channels of *UTIRAC* can be increase just by increasing the number of the selection clocks

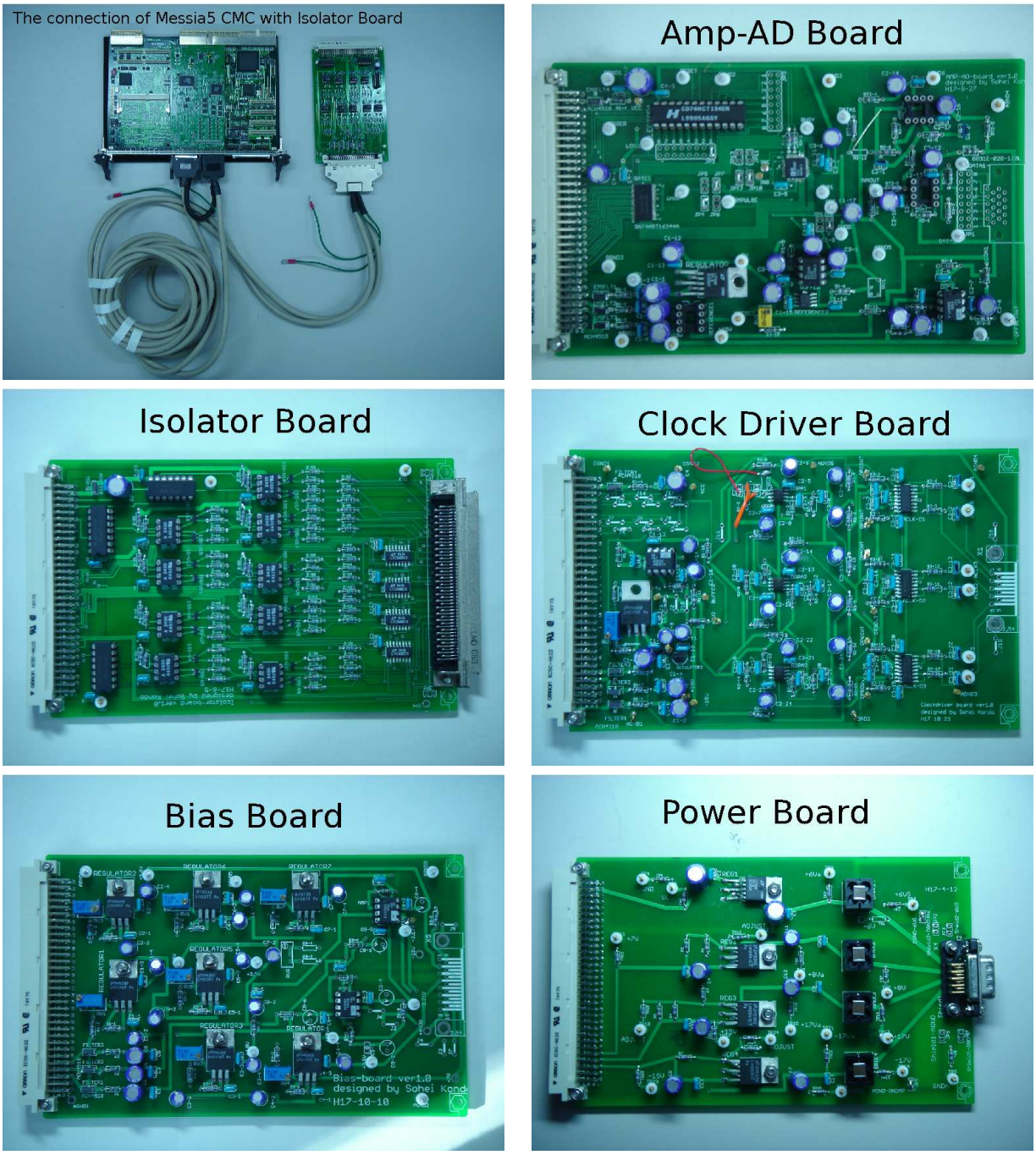

Figure 4. The *UTIRAC* boards.

3. CURRENT STATUS

We have described in details the newly developed array control system *UTIRAC*, which is based on MESSIA5 system. Working tests of each board and integration test with MESSIA5 system (for clock generation and frame acquisition) have been completed. ADC noise is confirmed to be equal to what is in the data-sheet. As a next step, we are going to test *VIRGO* MUX for operation with 4 outputs and to evaluate readout noise. In the near future, we will increase the number of input channels on a single Amp-AD board from one to four for the operation of arrays with 16 outputs.

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